FIG.1

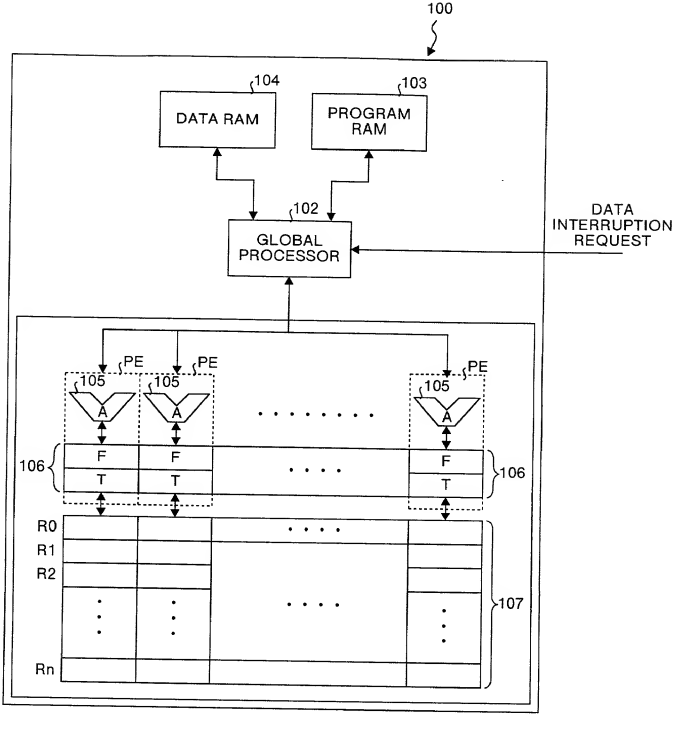

100
104
DATA RAM
103
PROGRAM RAM
102
GLOBAL PROCESSOR
DATA INTERRUPTION REQUEST
PE
105
A
F
T
106
R0
R1
R2
Rn
107

FIG.2

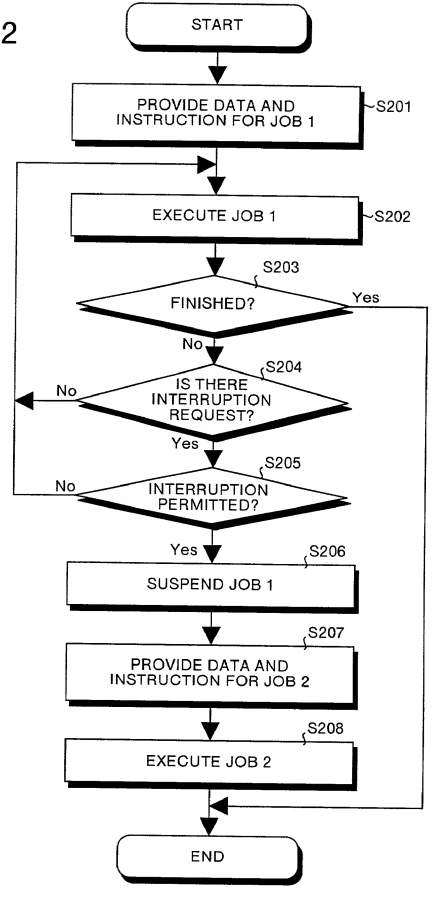

START
PROVIDE DATA AND INSTRUCTION FOR JOB 1
S201
EXECUTE JOB 1
S202
S203
FINISHED?
Yes
No
S204
IS THERE INTERRUPTION REQUEST?
No
Yes
S205
INTERRUPTION PERMITTED?
No
Yes
S206
SUSPEND JOB 1
S207
PROVIDE DATA AND INSTRUCTION FOR JOB 2
S208
EXECUTE JOB 2
END

FIG.3

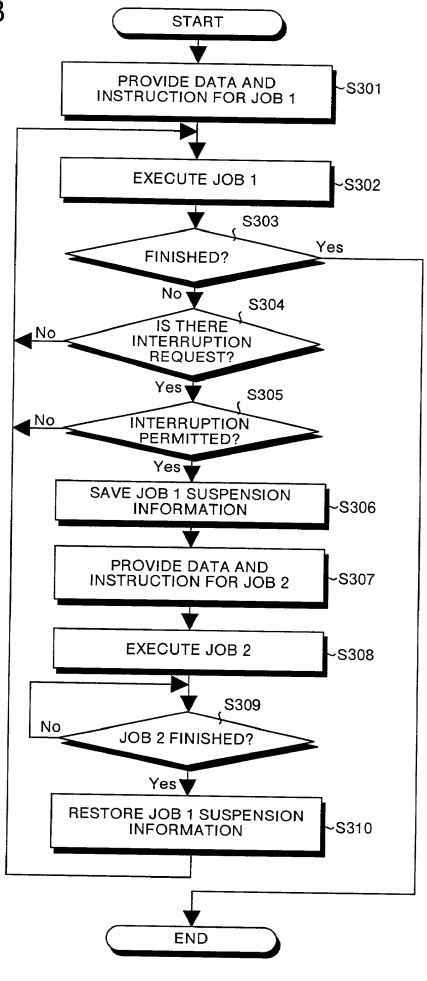

START
PROVIDE DATA AND INSTRUCTION FOR JOB 1
S301
EXECUTE JOB 1
S302
S303
FINISHED?
Yes
No
S304
IS THERE INTERRUPTION REQUEST?
No
Yes
S305
INTERRUPTION PERMITTED?
No
Yes
SAVE JOB 1 SUSPENSION INFORMATION
S306
PROVIDE DATA AND INSTRUCTION FOR JOB 2
S307
EXECUTE JOB 2
S308
S309
JOB 2 FINISHED?
No
Yes
RESTORE JOB 1 SUSPENSION INFORMATION
S310
END

FIG.4

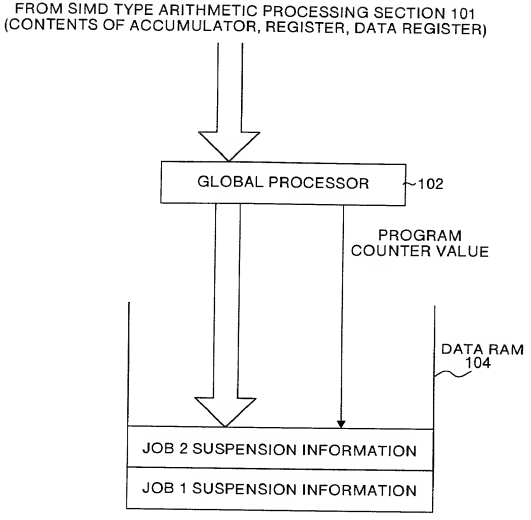

FROM SIMD TYPE ARITHMETIC PROCESSING SECTION 101
(CONTENTS OF ACCUMULATOR, REGISTER, DATA REGISTER)
GLOBAL PROCESSOR
102
PROGRAM
COUNTER VALUE
DATA RAM
104
JOB 2 SUSPENSION INFORMATION
JOB 1 SUSPENSION INFORMATION

FIG.5

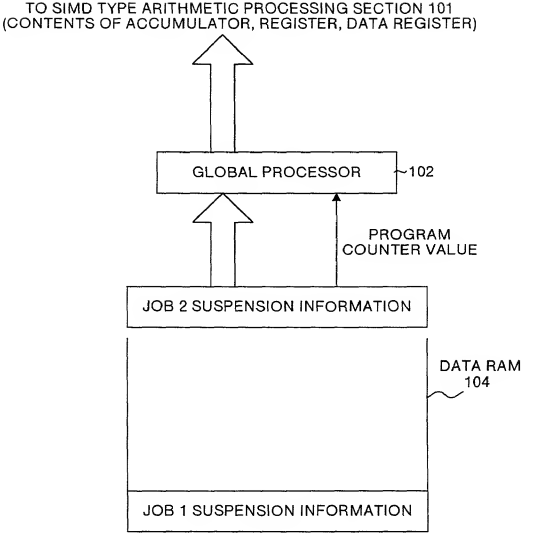

TO SIMD TYPE ARITHMETIC PROCESSING SECTION 101
(CONTENTS OF ACCUMULATOR, REGISTER, DATA REGISTER)
GLOBAL PROCESSOR
102
PROGRAM
COUNTER VALUE
JOB 2 SUSPENSION INFORMATION
DATA RAM
104
JOB 1 SUSPENSION INFORMATION

FIG.6

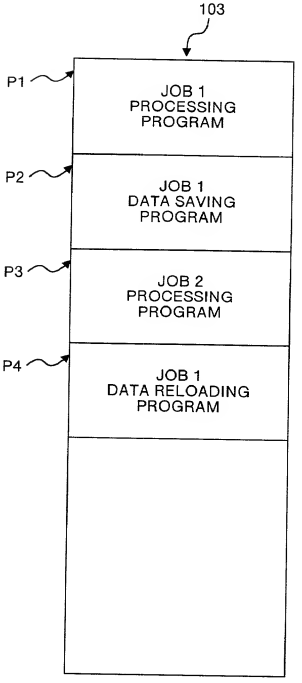

103
P1
JOB 1
PROCESSING
PROGRAM
P2
JOB 1
DATA SAVING
PROGRAM
P3
JOB 2
PROCESSING
PROGRAM
P4
JOB 1
DATA RELOADING
PROGRAM

FIG.7A

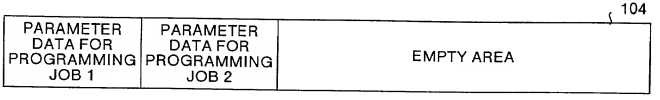
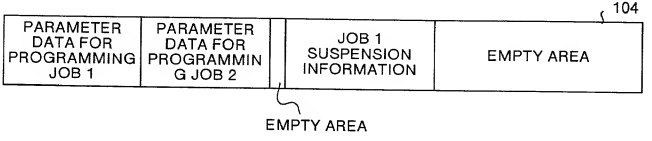
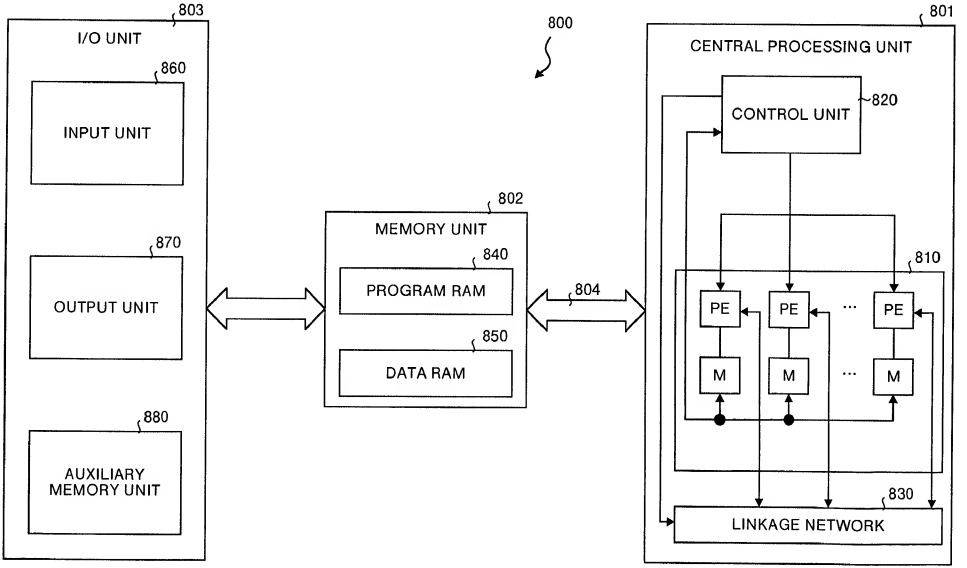

104
PARAMETER DATA FOR PROGRAMMING JOB 1
PARAMETER DATA FOR PROGRAMMING JOB 2
EMPTY AREA

FIG.7B


104
PARAMETER DATA FOR PROGRAMMING JOB 1
PARAMETER DATA FOR PROGRAMMIN G JOB 2
JOB 1 SUSPENSION INFORMATION
EMPTY AREA
EMPTY AREA

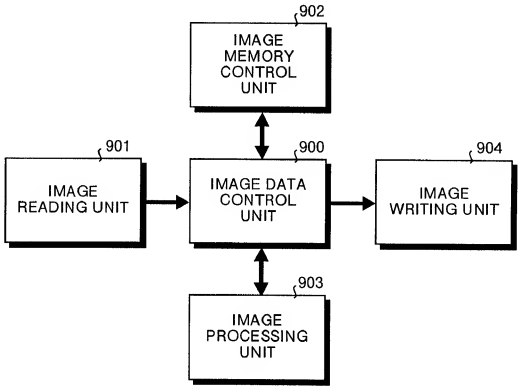
ORBLON, SPIVAK, ET AL.
DOCKET #:293930US6
INV.: Hiroaki FUKUDA, et al.
SHEET 8 OF 34

FIG.8



T060CD" EP07D860

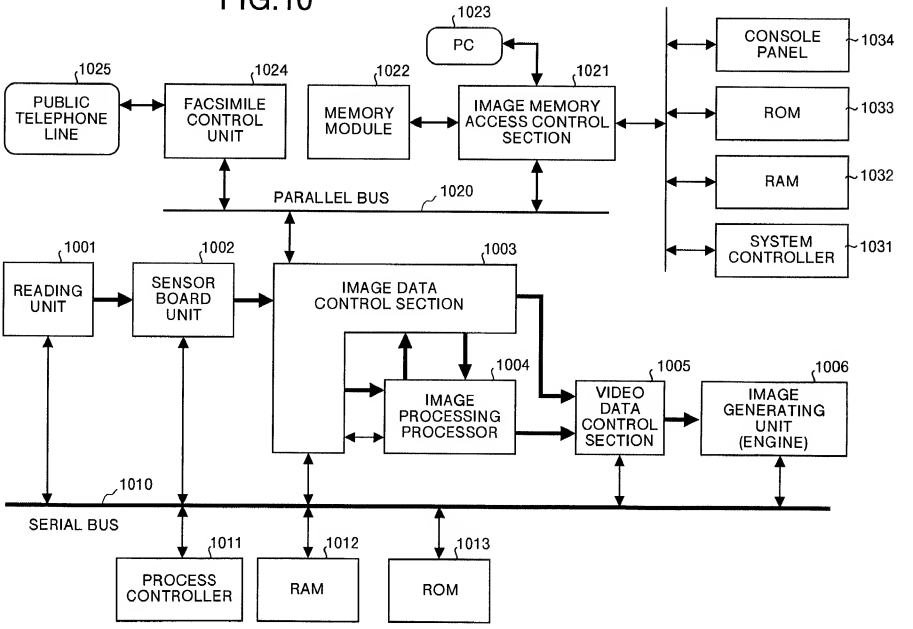
FIG.9



OBLON, SPIVAK, ET AL.
DOCKET #:203950US6
INVENTOR: Hiroaki FUKUDA, et al.
SHEET 9 OF 34
9/34

FOCCO "2H0F0860

FIG.10



OBLON, SPIVAK, ET AL.
DOCKET #:20930US6
INV.: Hiroaki FUKUDA, et al.
SHEET 10 OF 34

OBLON, SPIVAK, ET AL.
DOCKET #:20930U56
INV.: Hiroaki FUKUDA, et al.
SHEET 11 OF 34
11/34

FIG.11

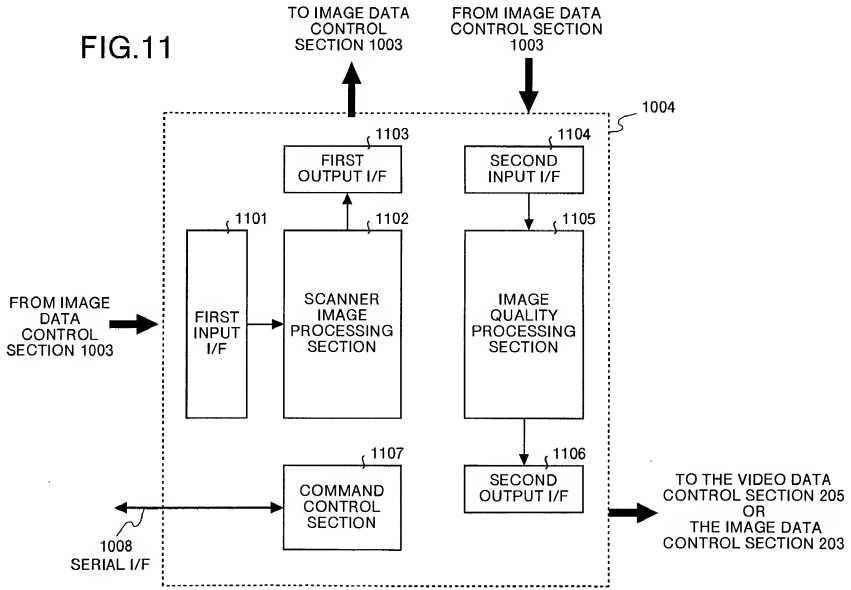


FIG.12

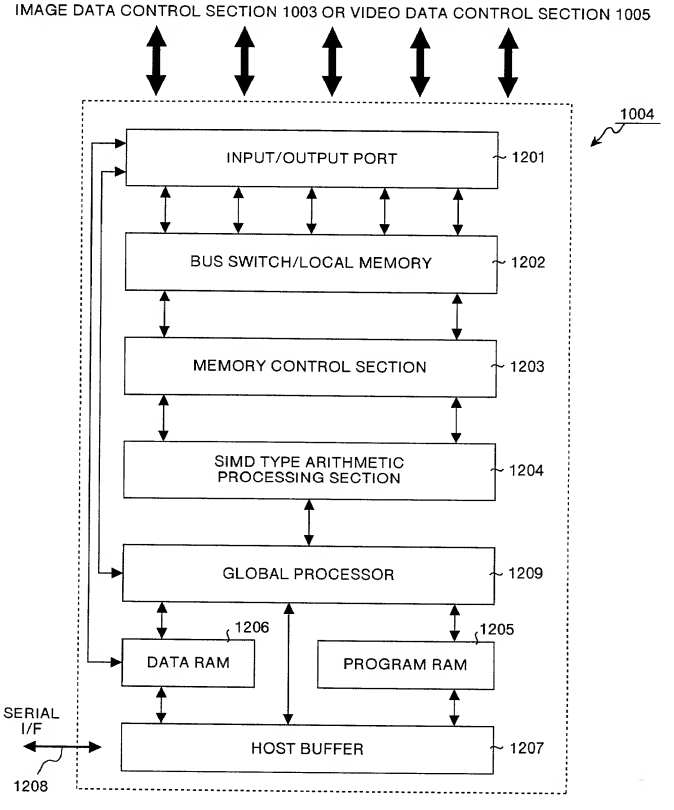
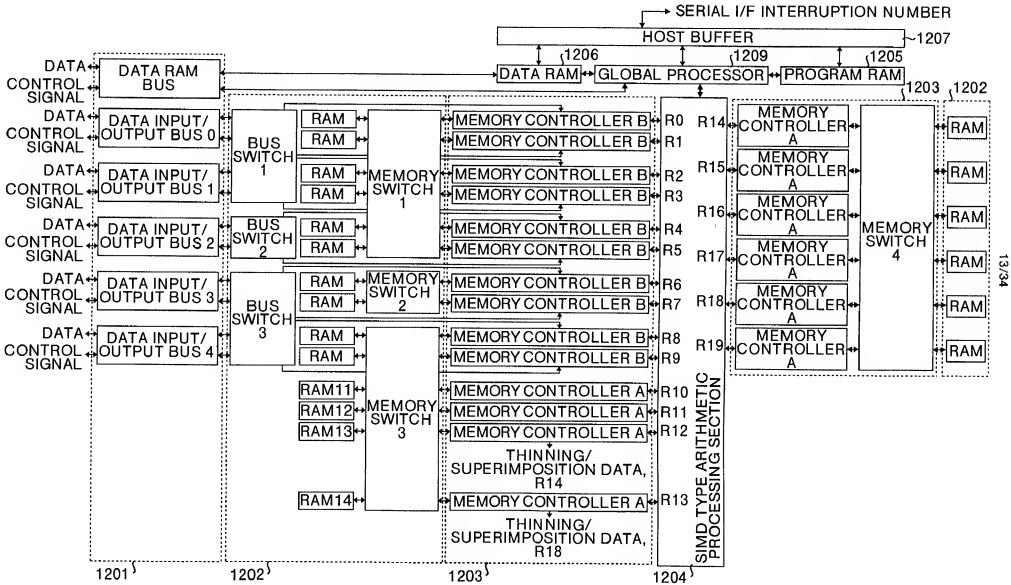


IMAGE DATA CONTROL SECTION 1003 OR VIDEO DATA CONTROL SECTION 1005
1004
INPUT/OUTPUT PORT
1201
BUS SWITCH/LOCAL MEMORY
1202
MEMORY CONTROL SECTION
1203
SIMD TYPE ARITHMETIC PROCESSING SECTION
1204
GLOBAL PROCESSOR
1209
1206
DATA RAM
1205
PROGRAM RAM
SERIAL I/F
HOST BUFFER
1207
1208

TOSOCO "EIBTOSOO

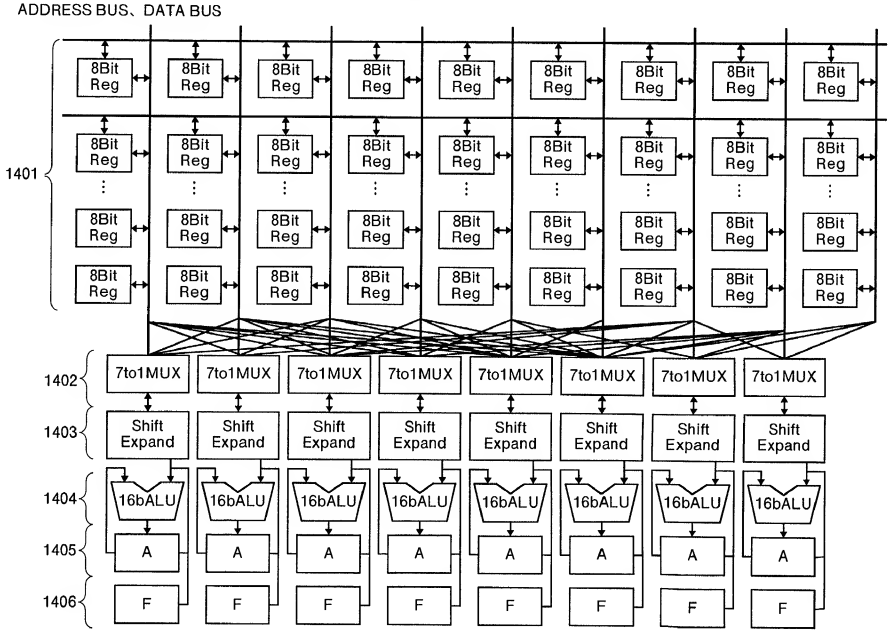
FIG.13



ORLON, SPIVAK, ET AL.
DOCKET #:2826/0356
INV: Hiroshi FUKUDA, et al.
SHEET 13 OF 34

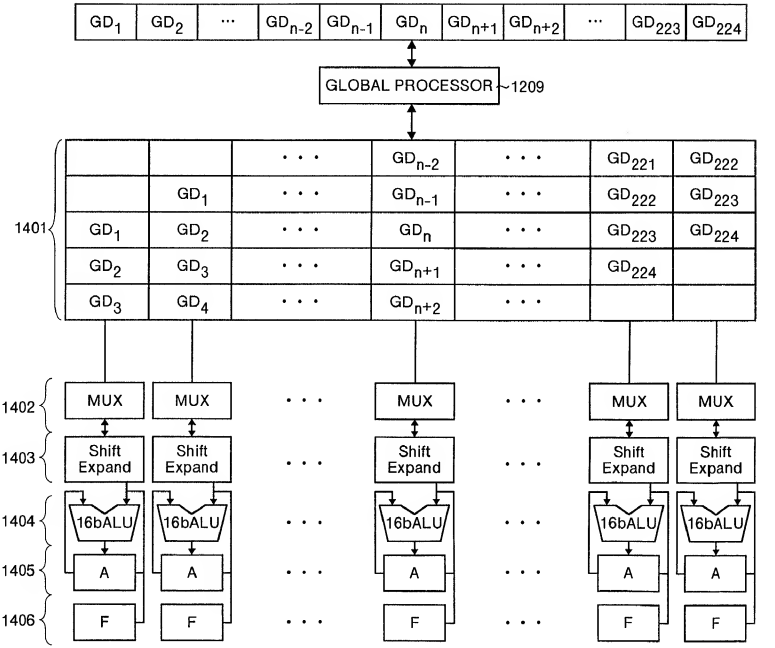
TOSHIBA Shibaura

FIG.14



OBLON, SPIVAK, ET AL.
DOCKET #:203930US6
INV: Hiroaki FUKUDA, et al.
SHEET 14 OF 34
14/34

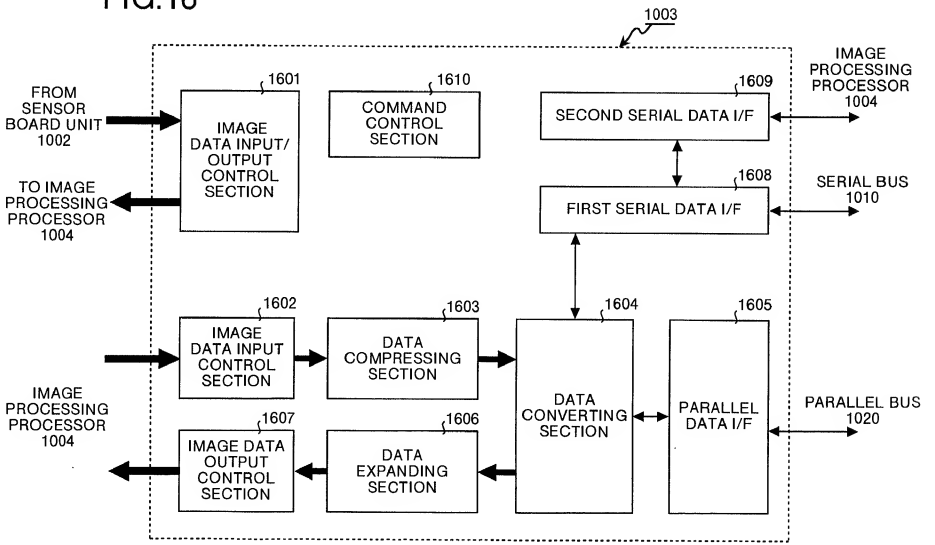
FIG.15



OBLON, SPIVAK, ET AL
DOCKET #:20930US6
INV: Hiroaki FUKUDA, et al.
SHEET 15 OF 34
15/34

FOSOEO"CL8TO860

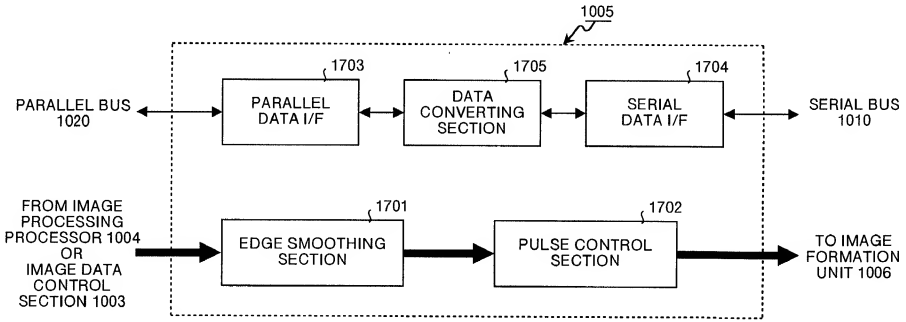
FIG.16



OBLON, SPIVAK, ET AL.
DOCKET #:203930US6
INV: Hiroaki FUKUDA, et al.
SHEET 16 OF 34

TOSHIBA CORPORATION

FIG.17



OBLON, SPIVAK, ET AL.
DOCKET #:203930US6
INV.: Hiroshi FUKUDA, et al.
SHEET 17 OF 34
17/34

FIG.18

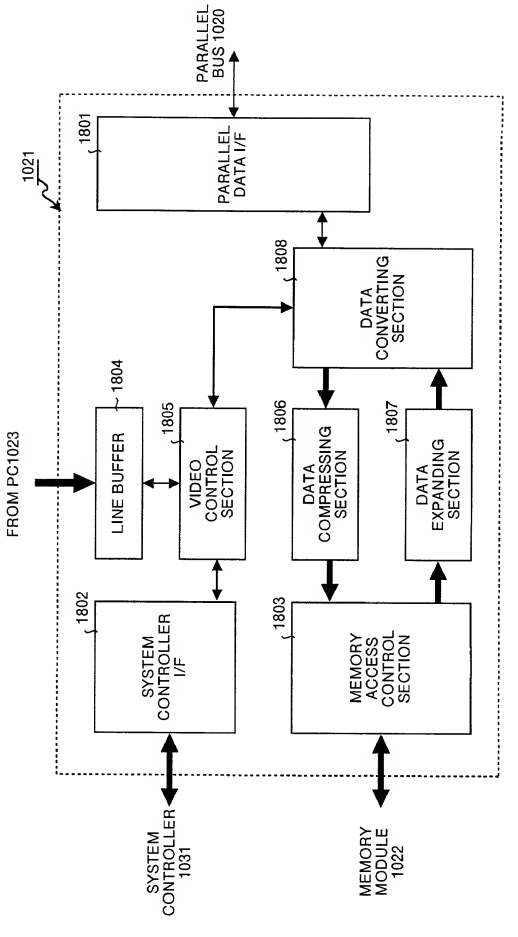

FROM PC1023
1021
LINE BUFFER
1804
VIDEO CONTROL SECTION
1805
SYSTEM CONTROLLER I/F
1802
MEMORY ACCESS CONTROL SECTION
1803
DATA COMPRESSING SECTION
1806
DATA EXPANDING SECTION
1807
DATA CONVERTING SECTION
1808
PARALLEL DATA I/F
1801
PARALLEL BUS 1020
SYSTEM CONTROLLER 1031
MEMORY MODULE 1022

FIG.19

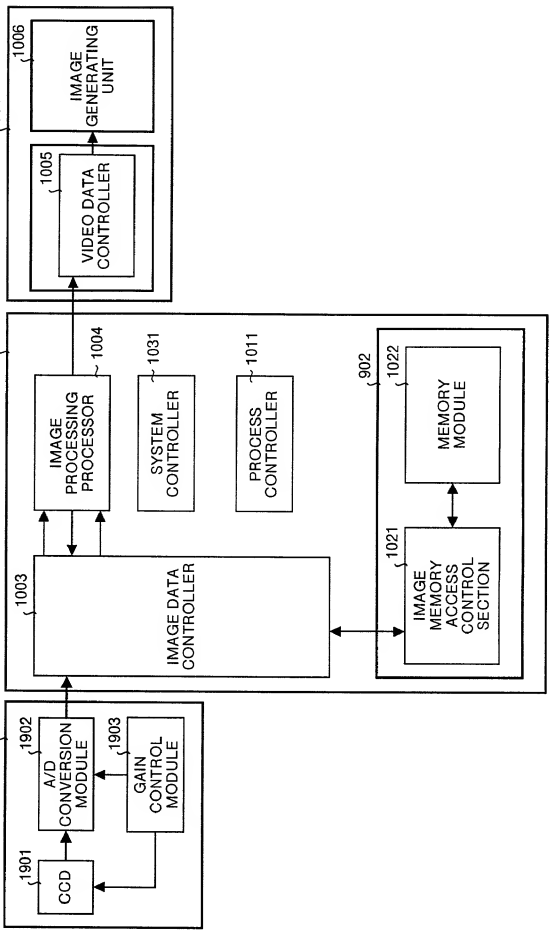
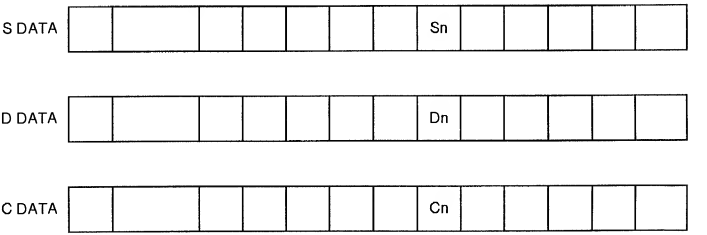

101
1901
CCD
1902
A/D CONVERSION MODULE
1903
GAIN CONTROL MODULE
1900
1003
IMAGE DATA CONTROLLER
1004
IMAGE PROCESSING PROCESSOR
1031
SYSTEM CONTROLLER
1011
PROCESS CONTROLLER
902
1021
IMAGE MEMORY ACCESS CONTROL SECTION
1022
MEMORY MODULE
904
1005
VIDEO DATA CONTROLLER
1006
IMAGE GENERATING UNIT

FIG.20

	j-2	j-1	COLUMN j	j+1	j+2
i-2	A	B	C	D	E
i-1	F	G	H	I	J
ROW i	K	L	M	N	O
i+1	P	Q	R	S	T
i+2	U	V	W	X	Y

OBLON, SPIVAK, ET AL
DOCKET #:2039US86
INV: Hiroaki FUKUDA, et al.
SHEET 21 OF 34

FIG.21



TOKUGI 2007-08-20

FIG.22

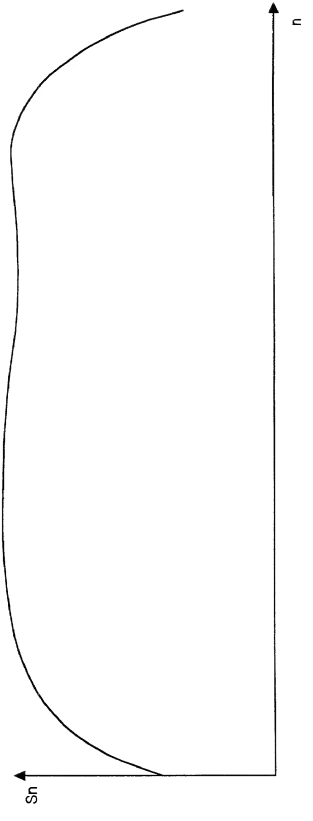


FIG.23

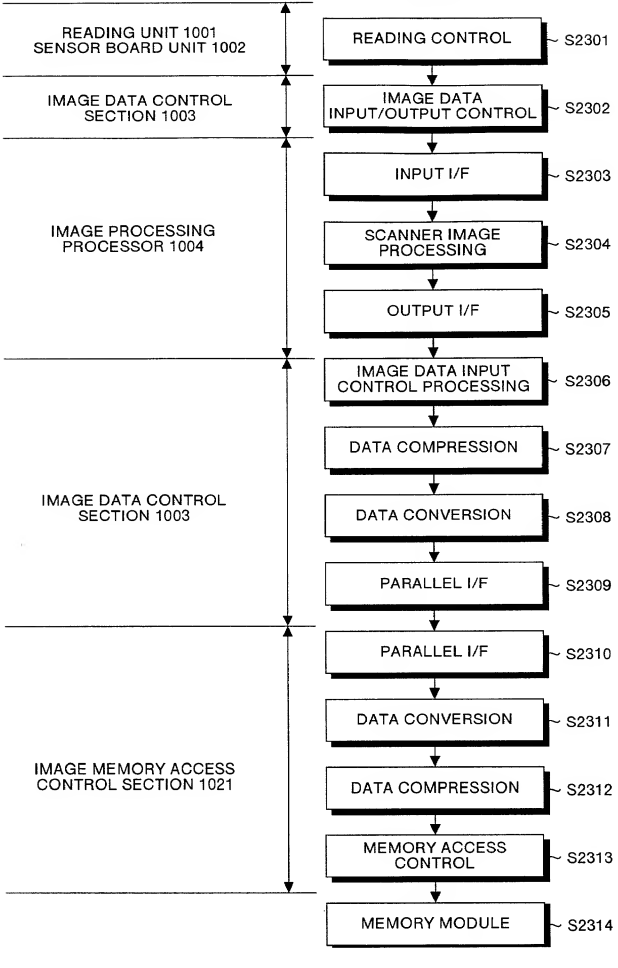

READING UNIT 1001
SENSOR BOARD UNIT 1002
IMAGE DATA CONTROL SECTION 1003
IMAGE PROCESSING PROCESSOR 1004
IMAGE DATA CONTROL SECTION 1003
IMAGE MEMORY ACCESS CONTROL SECTION 1021
READING CONTROL
S2301
IMAGE DATA INPUT/OUTPUT CONTROL
S2302
INPUT I/F
S2303
SCANNER IMAGE PROCESSING
S2304
OUTPUT I/F
S2305
IMAGE DATA INPUT CONTROL PROCESSING
S2306
DATA COMPRESSION
S2307
DATA CONVERSION
S2308
PARALLEL I/F
S2309
PARALLEL I/F
S2310
DATA CONVERSION
S2311
DATA COMPRESSION
S2312
MEMORY ACCESS CONTROL
S2313
MEMORY MODULE
S2314

FIG.24

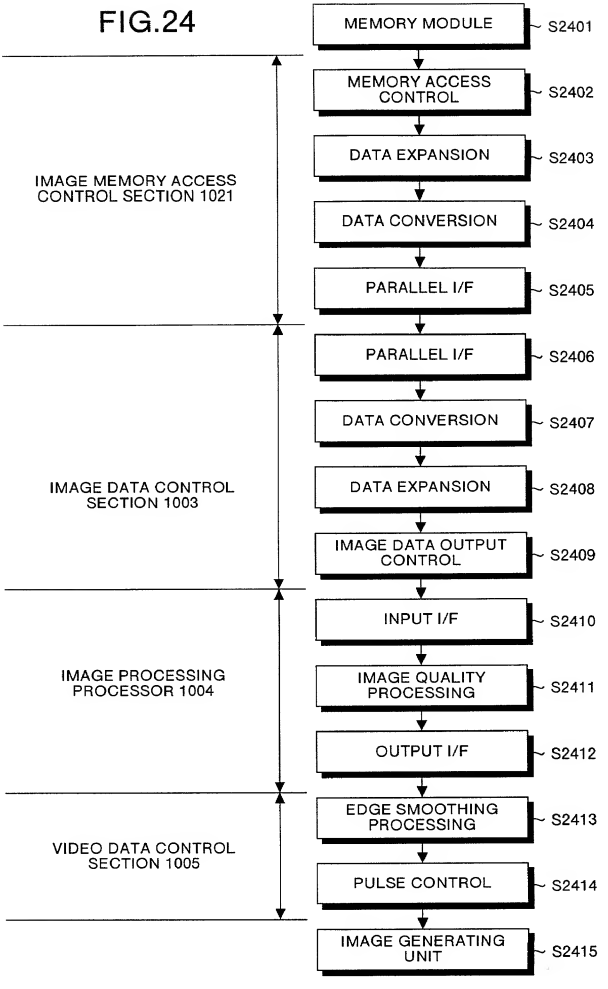


IMAGE MEMORY ACCESS CONTROL SECTION 1021
IMAGE DATA CONTROL SECTION 1003
IMAGE PROCESSING PROCESSOR 1004
VIDEO DATA CONTROL SECTION 1005
MEMORY MODULE
S2401
MEMORY ACCESS CONTROL
S2402
DATA EXPANSION
S2403
DATA CONVERSION
S2404
PARALLEL I/F
S2405
PARALLEL I/F
S2406
DATA CONVERSION
S2407
DATA EXPANSION
S2408
IMAGE DATA OUTPUT CONTROL
S2409
INPUT I/F
S2410
IMAGE QUALITY PROCESSING
S2411
OUTPUT I/F
S2412
EDGE SMOOTHING PROCESSING
S2413
PULSE CONTROL
S2414
IMAGE GENERATING UNIT
S2415

OBLON, SPIVAK, ET AL.
DOCKET #:220906US6
INV: Hitoshi FUKUDA, et al.
SHEET 25 OF 34

FIG.25

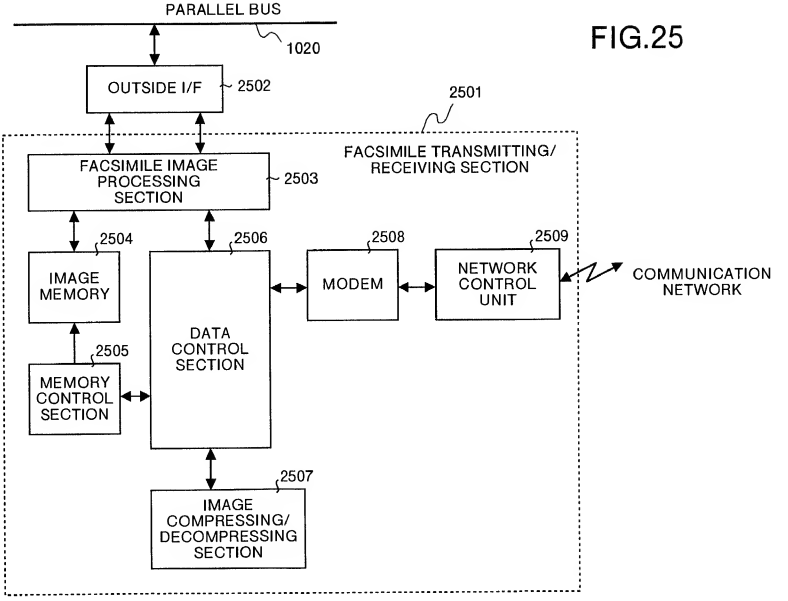
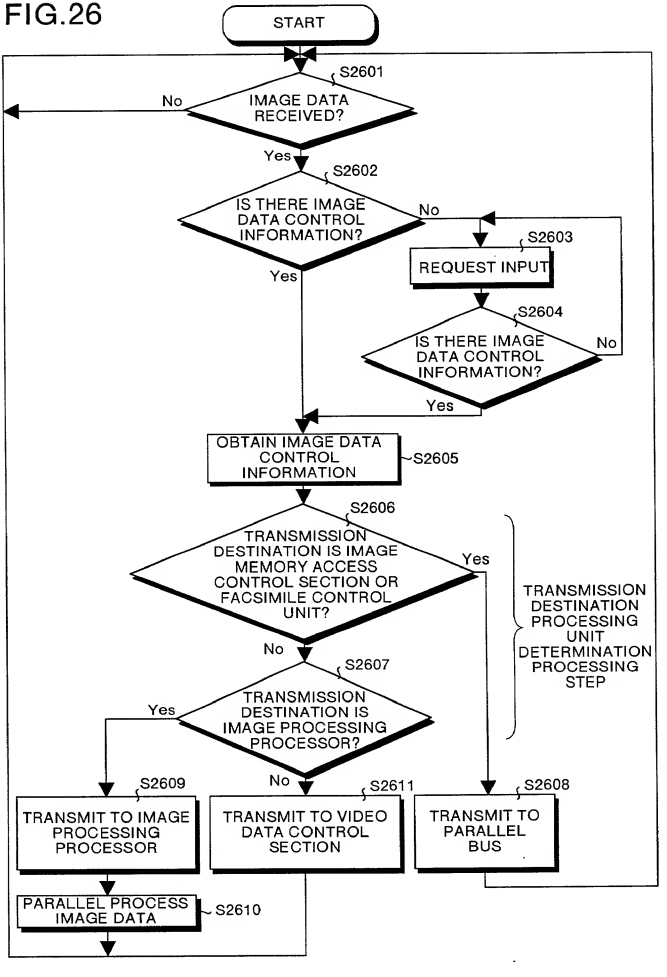


FIG.26


START
S2601
IMAGE DATA RECEIVED?
No
Yes
S2602
IS THERE IMAGE DATA CONTROL INFORMATION?
No
Yes
S2603
REQUEST INPUT
S2604
IS THERE IMAGE DATA CONTROL INFORMATION?
No
Yes
OBTAIN IMAGE DATA CONTROL INFORMATION
S2605
S2606
TRANSMISSION DESTINATION IS IMAGE MEMORY ACCESS CONTROL SECTION OR FACSIMILE CONTROL UNIT?
Yes
No
S2607
TRANSMISSION DESTINATION IS IMAGE PROCESSING PROCESSOR?
Yes
No
TRANSMISSION DESTINATION PROCESSING UNIT DETERMINATION PROCESSING STEP
S2609
TRANSMIT TO IMAGE PROCESSING PROCESSOR
S2611
TRANSMIT TO VIDEO DATA CONTROL SECTION
S2608
TRANSMIT TO PARALLEL BUS
PARALLEL PROCESS IMAGE DATA
S2610

ORLON, SPIVAK, ET AL.
DOCKET #203930US6
INV: Hiroaki FUKUDA, et al.
SHEET 27 OF 34
27/34

FIG.27

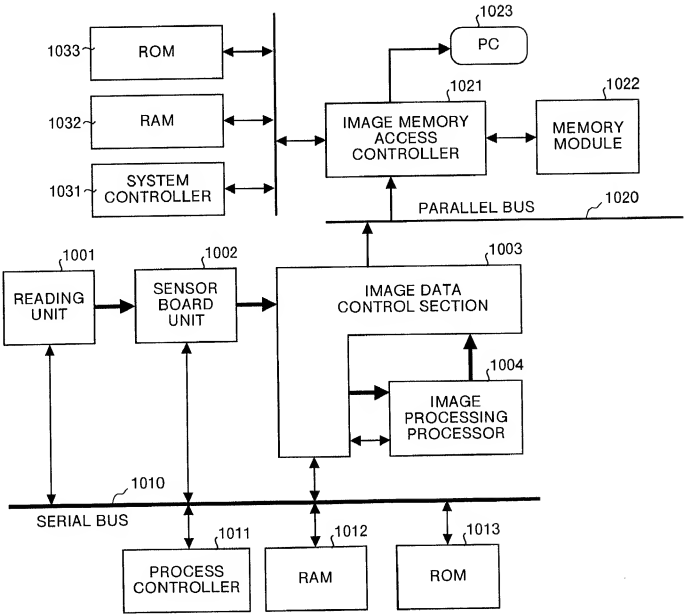
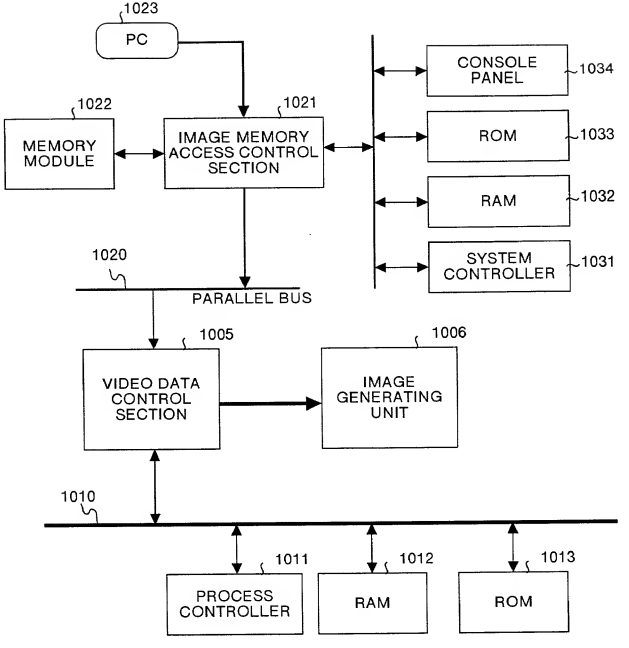
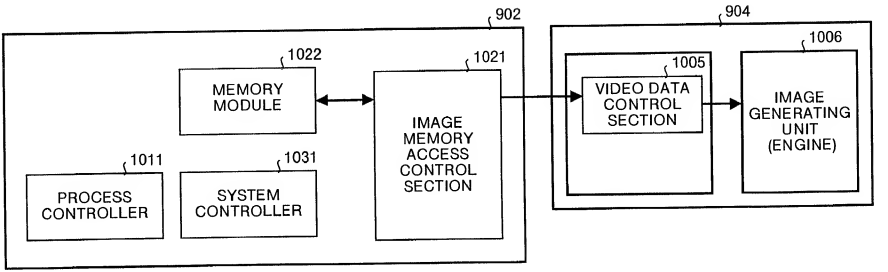


FIG.28


1023
PC
1022
MEMORY MODULE
1021
IMAGE MEMORY ACCESS CONTROL SECTION
CONSOLE PANEL
1034
ROM
1033
RAM
1032
SYSTEM CONTROLLER
1031
1020
PARALLEL BUS
1005
VIDEO DATA CONTROL SECTION
1006
IMAGE GENERATING UNIT
1010
1011
PROCESS CONTROLLER
1012
RAM
1013
ROM

TOSDEC "EP0810860

FIG.29



OBLON, SPIVAK, ET AL
DOCKET #20930US6
INV: Hiroaki FUKUDA, et al.
SHEET 29 OF 34

FIG.30

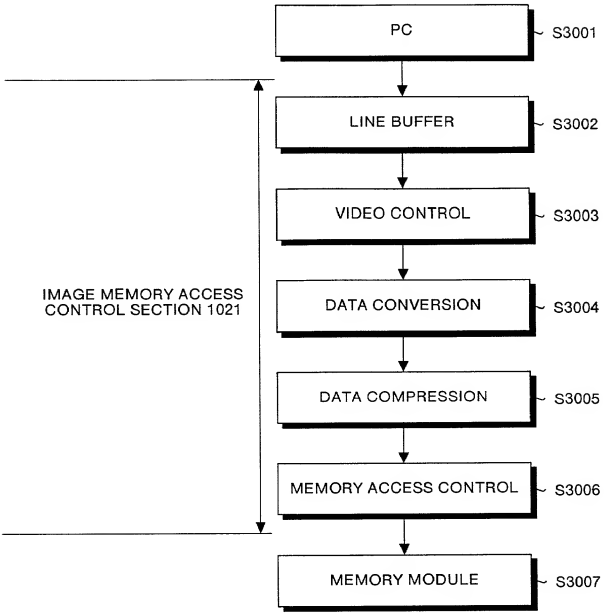
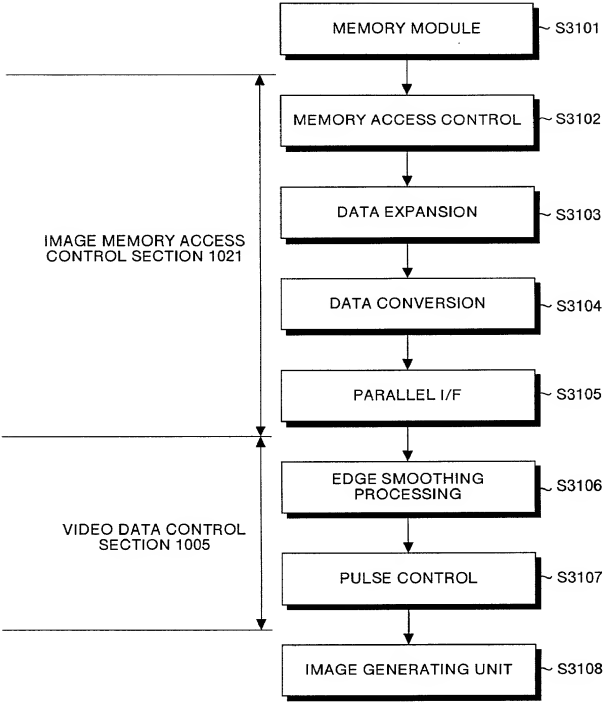
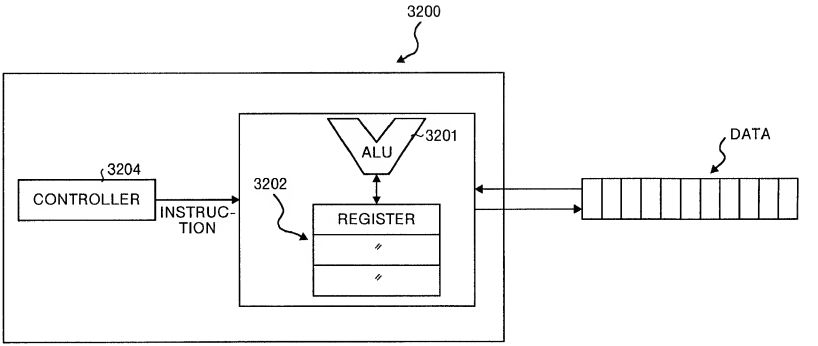

PC
S3001
LINE BUFFER
S3002
VIDEO CONTROL
S3003
IMAGE MEMORY ACCESS CONTROL SECTION 1021
DATA CONVERSION
S3004
DATA COMPRESSION
S3005
MEMORY ACCESS CONTROL
S3006
MEMORY MODULE
S3007

FIG.31


MEMORY MODULE
S3101
MEMORY ACCESS CONTROL
S3102
DATA EXPANSION
S3103
IMAGE MEMORY ACCESS CONTROL SECTION 1021
DATA CONVERSION
S3104
PARALLEL I/F
S3105
EDGE SMOOTHING PROCESSING
S3106
VIDEO DATA CONTROL SECTION 1005
PULSE CONTROL
S3107
IMAGE GENERATING UNIT
S3108

FD60CC0 C18TD8C0

FIG.32



ORLON, SPIVAK, ET AL.
DOCKET #2020US56
INV: Hiroshi FUKUDA, et al.
SHEET 32 OF 34

T06DCD" EA6TD86D

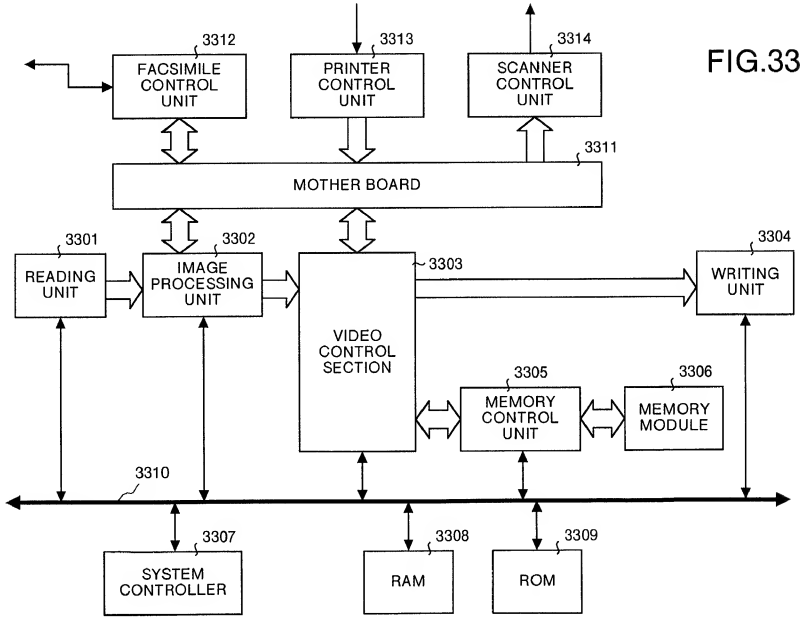
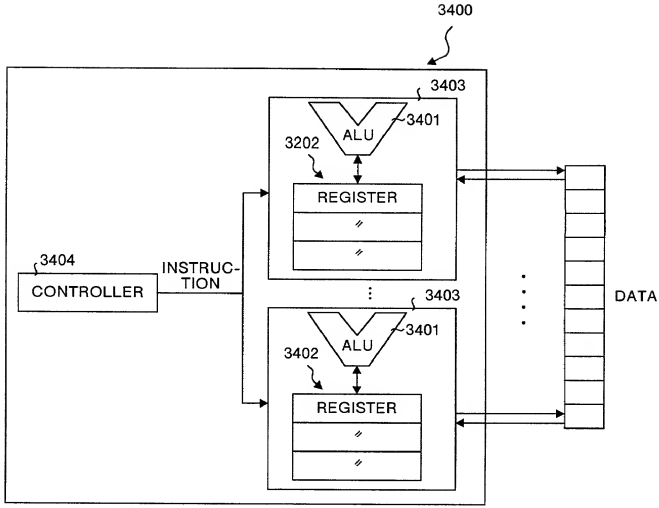


FIG.33

OBLON, SPIVAK, ET AL.
DOCKET #:20390US6
INV: Hiroaki FUKUDA, et al.
SHEET 33 OF 34

FIG.34


3400
3403
3401
ALU
3202
REGISTER
3404
CONTROLLER
INSTRUC-
TION
3403
3401
ALU
3402
REGISTER
DATA